

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side <sup>surfaces</sup> [surface] of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

C1  
Cont a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

P, 20 wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

---

C2 5 (Amended). A ferroelectric liquid crystal display device according to claim 1, wherein said semiconductor layer of said p-channel TFT has no LDD regions.

---

Sub D2  
Fig. 1 6 (Twice Amended). A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

C3 each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side <sup>surfaces</sup> [surface] of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said <sup>1st</sup> [second] source and drain regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

10 (Amended). A ferroelectric liquid crystal display device according to claim 6, wherein said semiconductor layer of said p-channel TFT has no LDD regions.

11 (Twice Amended). A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first gate electrode partially overlaps said first impurity region,

and

said p-channel TFT comprising:

C5  
cont. a second gate electrode formed adjacent to a second semiconductor layer with a second gate <sup>interposed therebetween</sup> insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region, wherein second gate electrode partially overlaps said third impurity region, and wherein a wiring is connected to said third impurity region.

C6 Sub FI 12 (Amended). A ferroelectric liquid crystal display device according to claim 11, wherein said first and second gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

14 (Twice Amended). A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

P.57  
fig. 150  
C7 each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side <sup>surfaces</sup> [surface] of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

C7  
cont. wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions.

C8 18 (Amended). A goggle type display device according to claim 14, wherein said semiconductor layer of said p-channel TFT has no LDD regions.

S257 19 (Twice Amended). A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side <sup>surfaces</sup> surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a pair of LDD regions and first source and drain regions; and

C9 a semiconductor layer of said p-channel TFT comprising a second channel formation region and second source and drain regions,

wherein a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein the portion which said second conductive layer is in contact with said gate insulating film in said n-channel <sup>TFT</sup> region does not overlap said first source and drain regions;

wherein a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlap said second source and drain regions.

C 10 23 (Amended). A goggle type display device according to claim 19, wherein said semiconductor layer of said p-channel TFT has no LDD regions.

24 (Twice Amended). A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

Sub D5 a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

C 11 wherein said first gate electrode partially overlaps said first impurity region, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, <sup>interposed therebetween</sup> said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said second gate electrode partially overlaps said third impurity region, and

wherein a wiring is connected to said third impurity region.

Sub F1 C 12 25 (Amended). A goggle type display device according to claim 24, wherein said first and second gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).